# **CSE 620: Advanced Computer Architecture**

# **Project: HDL Testbench**

**Digital System Modeling using HDL**

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* Include this header with your project.
* In doing this project, you could search the Internet, library, or any other source. ***Please do not copy material from your colleagues***.
* Total: **70 Marks**.

**Introduction:** In this project, you are required to do a set of HDL (VHDL or Verilog) mini-projects.

**Objective:** The objective of the assignment is to get the student experienced with HDL modeling and testbench creation.

**Scope:** Project scope includes developing HDL testbenches to a set of given non-trivial digital system designs.

**Statement:**

1. You are given:
   * The D-flip-flop testbench example, written in VHDL in the VHDL Overview module, included in the VHDL course that could be accessed on: https://sites.google.com/site/csevhdl.
   * An archive of the source code of all VHDL examples included in the VHDL course above. The archive is in the “VHDL Code Examples” folder on the “Course Material” page on the site mentioned above.
2. Select a number of the given example designs in the given archive and develop testbenches to them similar to the D-flip-flop testbench mentioned above.
3. You need to decide whether to do the mini-projects in VHDL or Verilog:
   * **VHDL option**: select 10 example designs.
   * **Verilog option**: select 5 example designs. You need to convert them to Verilog first, and then develop testbenches to them.

**Deadline:** Assignment starts from the first day of the term. The documentation submission and source code email are required before the starting time of the course final exam. No submission will be accepted after that time.

**Deliverables:** A documentation for all mini-projects and an archive of the source code of all developed testbenches. The source code archive is to be emailed to the course instructor. The documentation should include the following (at least) for each design:

1. Design example name and location in the slides,
2. If you are doing the project in Verilog, include and document the code of the design example,
3. Test strategy,
4. Testbench code,
5. Documentation for the testbench code,
6. Simulation results with comments, and
7. Names of all used tools.

**Notes:**

* The final documentation should be well written from the language and organization points of view. It must be precise and concise.
* Support the final documentation with neat diagrams and tables.
* Include a good list of references in the final documentation. Please cite every resource you use.
* To save you time, you do not need to reproduce figures/illustrations from resources. You could copy them as they are, if you wish. In that case, you must associate the copied material with a reference.
* Mini-projects are to be done individually. No groups are permitted.
* Do not copy testbenches and reports from your colleagues. Partially or fully copied testbenches or reports get zero credit.

***End of Assignment***